MQBG1D5-DMC-T1

Features

- Up to 28Gbps Data rate per channel
- 4 channels 1310nm DFB
- Maximum link length of 500m on G.652 SMF
- Electrically hot-pluggable
- Case operating temperature range:0°C to +70°C
- Power dissipation <3.5 W
- Single MPO connector receptacle

Applications

- 100G Ethernet links
- Infiniband DDR/EDR
- Datacenter and Enterprise networking

Standards

- Compliant with QSFP28 MSA
- Compliant with SFF-8636
- RoHS Compliant

General Description

MQBG1D5-DMC-T1 is a Four-Channel, Pluggable, Parallel, Fiber-Optic QSFP28 PSM4 for 100 Gbps Ethernet, Infiniband DDR/EDR applications. This transceiver is a high performance module for data communication and interconnect applications. It integrates four data lanes in each direction with 104Gbps bandwidth. Each lane can operate at 28Gbps up to 500m over G.652 SMF. These modules are designedto operate over singlemode fiber systems using a nominal wavelength of 1310nm. The electrical interface uses a 38 contact edge type connector. The optical interface uses an 12 fiber MTP (MPO) connector.

Specification

Absolute Maximum Ratings						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Note**
Storage Temperature	Ts	-20	-	85	℃	
Relative Humidity	RH	5	-	95	%	
Power Supply Voltage	VCC	-0.3	-	3.6	V	
Signal Input Voltage		-0.3	-	Vcc+0.3	V	

Recommended Operating Conditions						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Note**
Case Operating Temperature	Tcase	0	-	70	℃	Without air flow
Power Supply Voltage	VCC	3.13	3.3	3.47	V	
Power Supply Current	ICC	-		1.1	A	
Data Rate	BR		25.78125		Gbps	Each channel
Transmission Distance	TD		-	500	m	G.652 SMF

Optical Characteristics						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**NOTE**
Transmitter						
Center Wavelength	λ0	1295	1310	1325	nm	
Average Launch Power each lane	P_{AVG}	-9.4		2	dBm	
OMA, each Lane	P_{OMA}			2.2	dBm	1
SRMS	SMSR	30			dB	
Optical Extinction Ratio	ER	3.5			dB	
Transmitter and Dispersion Penalty each lane	TDP			2.9	dB	
Optical Return Loss To lerance	ORL			20	dB	
Transmitter Reflectance	R_T			-12	dB	
Output Eye Mask coordinates:{X1, X2, X3, Y1, Y2, Y3}	{0.31,0.4,0.45,0.34,0.38,0.4}					Hit Ratio = 5x10-5
Receiver						
Receiver Wavelength	λin	1295	1310	1325	nm	
Damage Threshold,each lane	THd	3			dBm	2
Average Receive Power,each lane	RSENS	-12.66		2	dBm	
Receiver Sensitivity (Average power)	Psen			-11.5	dBm	3
Receiver Sensitivity (OMA),each lane				-9	dBm	4
LOS Assert	LOSA	-30	-18		dBm	
LOS De-Assert	LOSD		-15	-7.5	dBm	
LOS Hysteresis		0.5			dB	
Input Saturation Power (Overload)	Psat	3.5			dBm	
Receiver Reflectance	Rr			-26	dB	

Notes:

1. Even if the TDP<1dB,the OMA min must exceed the minimum value specified here
2. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having thispower level on one lane. The receiver does not have to operate correctly at this input power.

3. Receiver Sensitivity(Average power) measured with a PRBS 2^{31}-1 test pattern, @25.78125Gb/s, BER<1E-12.
4. Receiver Sensitivity(OMA) measured with a PRBS 2^{31}-1 test pattern, @25.78125Gb/s, BER<5E-5.

Electrical Characteristics						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**NOTE**
Supply Voltage	Vcc	3.13	3.3	3.47	V	
Supply Current	Icc			1.1	A	
Transmitter						
Input differential impedance	Z_{IN}	90	100	110	Ω	
Differential data input swing	Vin,pp	190		900	mV_{PP}	1
Single ended input voltage tolerance	VinT	-0.3		4.0	V	
Receiver						
Single ended output voltage tolerance	VoutT	-0.3		4.0	V	
Differential Output impedance	Z_{OUT}	90	100	110	Ω	
Differential data output swing	Vout,pp	300		850	mV_{PP}	2

Notes:

1. Differential data input swing is measured between TxnP and TxnN.

2. Differential data output swing is measured between RxnP and RxnN

Pin Assignment

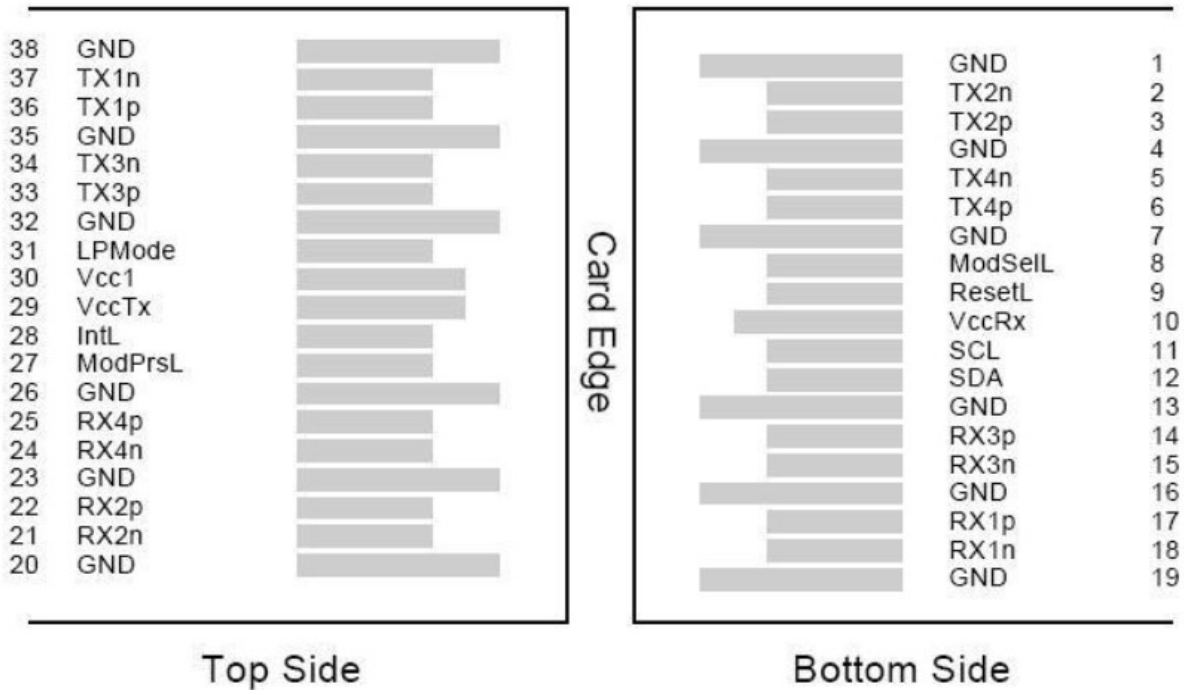


Figure 1---Pinout of Connector Block on Host Board

Pin	Symbol	Name/Description	NOTE
1	GND	Transmitter Ground (Common with Receiver Ground)	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data output	
4	GND	Transmitter Ground (Common with Receiver Ground)	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data output	
7	GND	Transmitter Ground (Common with Receiver Ground)	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	VccRx	3.3V Power Supply Receiver	2
11	SCL	2-Wire serial Interface Clock	
12	SDA	2-Wire serial Interface Data	
13	GND	Transmitter Ground (Common with Receiver Ground)	
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Transmitter Ground (Common with Receiver Ground)	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	

19	GND	Transmitter Ground (Common with Receiver Ground)	1
20	GND	Transmitter Ground (Common with Receiver Ground)	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Transmitter Ground (Common with Receiver Ground)	1
24	Rx4n	Receiver Inverted Data Output	1
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Transmitter Ground (Common with Receiver Ground)	1
27	ModPrsl	Module Present	
28	IntL	Interrupt	
29	VccTx	3.3V power supply transmitter	2
30	Vcc1	3.3V power supply	2
31	LPMode	Low Power Mode，not connect	
32	GND	Transmitter Ground (Common with Receiver Ground)	1
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Output	
35	GND	Transmitter Ground (Common with Receiver Ground)	1
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Output	
38	GND	Transmitter Ground (Common with Receiver Ground)	1

Notes:

1. GND is the symbol for signal and supply (power) common for QSFP28 modules. All are common within the QSFP28 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.

2. VccRx, Vcc1 and VccTx are the receiving and transmission power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP28 transceiver module in any combination. The connector pins are each rated for a maximum current of 500mA.

Digital Diagnostic Functions

MNC MQBG1D5-DMC-T1 support the 2-wire serial communication protocol as defined in the QSFP28 MSA, which allows real-time access to the following operating parameters:

- Transceiver temperature
- Laser bias current
- Transmitted optical power
- Received optical power
- Transceiver supply voltage

It also provides a sophisticated system of alarm and warning flags, which may be used to alert end-users when particular operating parameters are outside of a factory-set normal range.

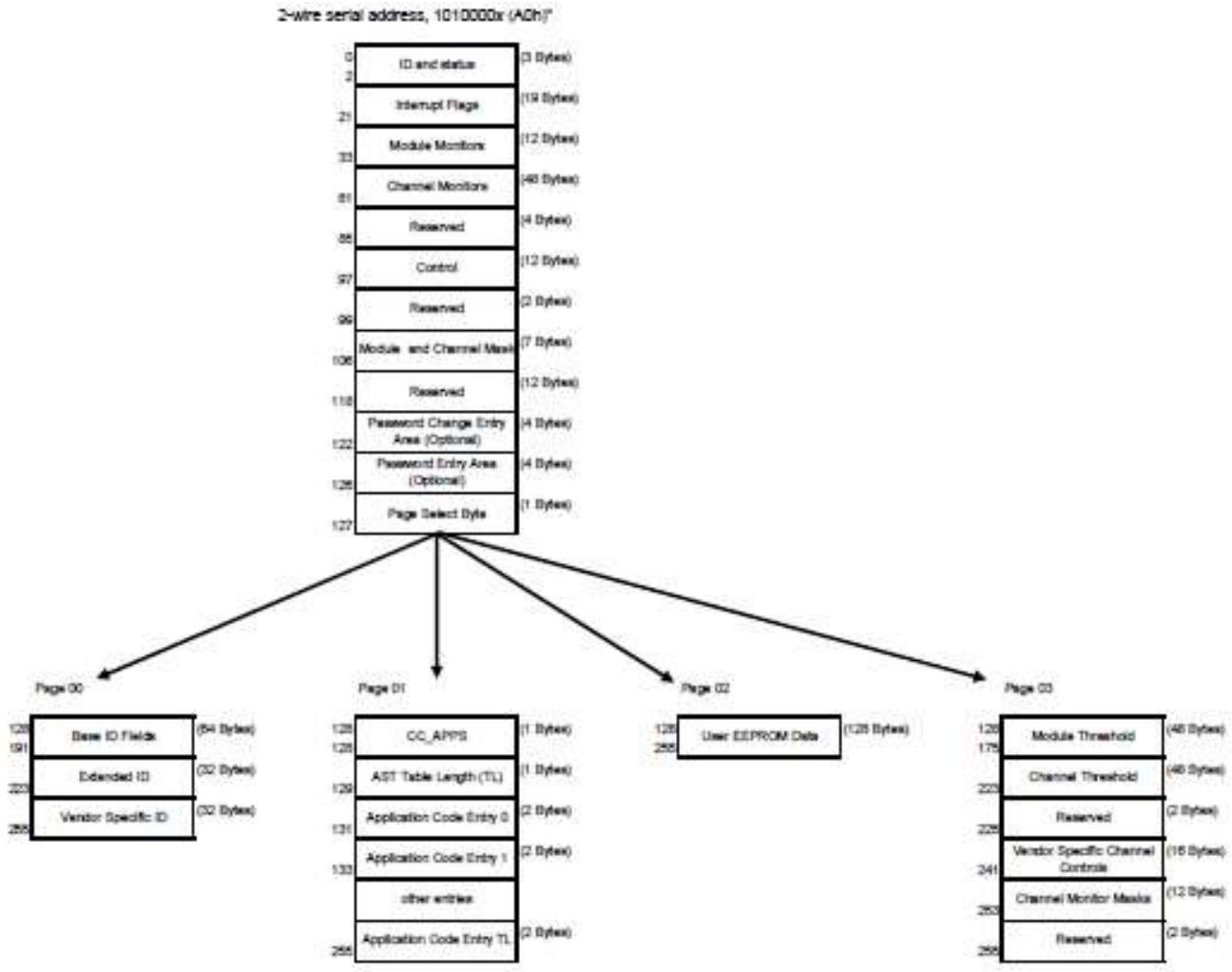
The operating and diagnostics information is monitored and reported by a Digital Diagnostics Transceiver Controller inside the transceiver, which is accessed through the 2-wire serial interface. When the serial protocol is activated, the serial clock signal (SCL pin) is generated by the host. The positive edge clocks data into the QSFP28 transceiver into those segments of its memory map that are not write-protected. The negative edge clocks data from the QSFP28 transceiver. The serial data signal (SDA pin) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially. The 2-wire serial interface provides sequential or random access to the 8 bit parameters, addressed from 00h to the maximum address of the memory.

This clause defines the Memory Map for QSFP28 transceiver used for serial ID, digital monitoring and certain control functions. The interface is mandatory for all QSFP28 devices. The memory map has been changed in order to accommodate 4 optical channels and limit the required memory space. The structure of the memory is shown in Figure 2 -QSFP28 Memory Map. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access toaddresses in the lower page, e.g. Interrupt Flags and Monitors. Less time critical entries, e.g. serial IDinformation and threshold settings, are

available with the Page Select function. The structure also provides address expansion by adding additional upper pages as needed. For example, in Figure 2 upper pages 01 and 02 are optional. Upper page 01 allows implementation of Application Select Table, and upper page 02 provides user read/write space.The lower page and upper pages 00 and 03 are always implemented. The interface address used is A0xh and is mainly used for time critical data like interrupt handling in order to enable a “one-time-read” for all data related to an interrupt situation. After an Interrupt, IntL, has been asserted, the host can read out the flag field to determine the effected channel and type of flag.

For more detailed information including memory map definitions, please see the QSFP28 MSA Specification.

Figure 2 –QSFP28 Memory Map



Lower Memory Map

The lower 128 bytes of the 2-wire serial bus address space, see Table 1, is used to access a variety of measurements and diagnostic functions, a set of control functions, and a means to select which of the varioussupper memory map pages are accessed on subsequent reads. This portion of the address space is alwaysdirectly addressable and thus is chosen for monitoring and control functions that may need to be repeatedlyaccessed. The definition of identifier field is the same as page 00h Byte 128.

Table 1— Lower Memory Map

Byte Address	Description	Type
0	Identifier (1 Byte)	Read-Only
1-2	Status (2 Bytes)	Read-Only
3-21	Interrupt Flags (19 Bytes)	Read-Only
22-33	Module Monitors (12 Bytes)	Read-Only
34-81	Channel Monitors (48 Bytes)	Read-Only
82-85	Reserved (4 Bytes)	Read-Only
86-97	Control (12 Bytes)	Read/Write
98-99	Reserved (2 Bytes)	Read/Write
100-106	Module and Channel Masks (7 Bytes)	Read/Write
107-118	Reserved (12 Bytes)	Read/Write
119-122	Password Change Entry Area (optional) (4 Bytes)	Read/Write
123-126	Password Entry Area (optional) (4 Bytes)	Read/Write
127	Page Select Byte	Read/Write

Status Indicator Bits

The Status Indicators are defined in Table 2.

Table 2 — Status Indicators

Byte	Bit	Name	Description
1	All	Reserved	
2	7	Reserved	
	6	Reserved	
	5	Reserved	
	4	Reserved	
	3	Reserved	
	2	Reserved	
	1	IntL	Digital state of the IntL interrupt output pin.
	0	Data_Not_Ready	Indicates transceiver has not yet achieved power up and monitor data is not ready. Bit remains high until data is ready to be read at which timethe device sets the bit low.

Interrupt Flags

A portion of the memory map (Bytes 3 through 21), form a flag field. Within this field, the status of LOS and TxFault as well as alarms and warnings for the various monitored items is reported. For normal operation anddefault state, the bits in this field have the value of 0b. For the defined conditions of LOS, Tx Fault, moduleand channel alarms and warnings, the appropriate bit or bits are set, value = 1b. Once asserted, the bits remained set (latched) until cleared by a read operation that includes the affected bit or reset by the ResetLpin.The Channel Status Interrupt Flags are defined in Table 3.

Table 3 — Channel Status Interrupt Flags

Byte	Bit	Name	Description
3	7	L-Tx4 LOS	Latched TX LOS indicator, channel 4 (Not support)
	6	L-Tx3 LOS	Latched TX LOS indicator, channel 3 (Not support)
	5	L-Tx2 LOS	Latched TX LOS indicator, channel 2 (Not support)
	4	L-Tx1 LOS	Latched TX LOS indicator, channel 1 (Not support)
	3	L-Rx4 LOS	Latched RX LOS indicator, channel 4
	2	L-Rx3 LOS	Latched RX LOS indicator, channel 3
	1	L-Rx2 LOS	Latched RX LOS indicator, channel 2
	0	L-Rx1 LOS	Latched RX LOS indicator, channel 1
4	7-4	Reserved	
	3	L-Tx4 Fault	Latched TX fault indicator, channel 4
	2	L-Tx3 Fault	Latched TX fault indicator, channel 3
	1	L-Tx2 Fault	Latched TX fault indicator, channel 2
	0	L-Tx1 Fault	Latched TX fault indicator, channel 1
5	All	Reserved	

The Module Monitor Interrupt Flags are defined in Table 4.

Table 4 — Module Monitor Interrupt Flags

Byte	Bit	Name	Description
6	7	L-Temp High Alarm	Latched high temperature alarm
	6	L-Temp Low Alarm	Latched low temperature alarm
	5	L-Temp High Warning	Latched high temperature warning
	4	L-Temp Low Warning	Latched low temperature warning
	3-0	Reserved	
7	7	L-Vcc High Alarm	Latched high supply voltage alarm
	6	L-Vcc Low Alarm	Latched low supply voltage alarm
	5	L-Vcc High Warning	Latched high supply voltage warning
	4	L-Vcc Low Warning	Latched low supply voltage warning
	3-0	Reserved	
8	All	Reserved	

The Channel Monitor Interrupt Flags are defined in Table 5

Table 5 — Channel Monitor Interrupt Flags

Byte	Bit	Name	Description
9	7	L-Rx1 Power High Alarm	Latched high RX power alarm, channel 1
	6	L-Rx1 Power Low Alarm	Latched low RX power alarm, channel 1
	5	L-Rx1 Power High Warning	Latched high RX power warning, channel 1
	4	L-Rx1 Power Low Warning	Latched low RX power warning, channel 1
	3	L-Rx2 Power High Alarm	Latched high RX power alarm, channel 2
	2	L-Rx2 Power Low Alarm	Latched low RX power alarm, channel 2
	1	L-Rx2 Power High Warning	Latched high RX power warning, channel 2
	0	L-Rx2 Power Low Warning	Latched low RX power warning, channel 2
10	7	L-Rx3 Power High Alarm	Latched high RX power alarm, channel 3
	6	L-Rx3 Power Low Alarm	Latched low RX power alarm, channel 3
	5	L-Rx3 Power High Warning	Latched high RX power warning, channel 3
	4	L-Rx3 Power Low Warning	Latched low RX power warning, channel 3
	3	L-Rx4 Power High Alarm	Latched high RX power alarm, channel 4
	2	L-Rx4 Power Low Alarm	Latched low RX power alarm, channel 4
	1	L-Rx4 Power High Warning	Latched high RX power warning, channel 4
	0	L-Rx4 Power Low Warning	Latched low RX power warning, channel 4
11	7	L-Tx1 Bias High Alarm	Latched high TX bias alarm, channel 1
	6	L-Tx1 Bias Low Alarm	Latched low TX bias alarm, channel 1
	5	L-Tx1 Bias High Warning	Latched high TX bias warning, channel 1
	4	L-Tx1 Bias Low Warning	Latched low TX bias warning, channel 1
	3	L-Tx2 Bias High Alarm	Latched high TX bias alarm, channel 2
	2	L-Tx2 Bias Low Alarm	Latched low TX bias alarm, channel 2
	1	L-Tx2 Bias High Warning	Latched high TX bias warning, channel 2
	0	L-Tx2 Bias Low Warning	Latched low TX bias warning, channel 2
12	7	L-Tx3 Bias High Alarm	Latched high TX bias alarm, channel 3
	6	L-Tx3 Bias Low Alarm	Latched low TX bias alarm, channel 3
	5	L-Tx3 Bias High Warning	Latched high TX bias warning, channel 3
	4	L-Tx3 Bias Low Warning	Latched low TX bias warning, channel 3
	3	L-Tx4 Bias High Alarm	Latched high TX bias alarm, channel 4
	2	L-Tx4 Bias Low Alarm	Latched low TX bias alarm, channel 4
	1	L-Tx4 Bias High Warning	Latched high TX bias warning, channel 4
	0	L-Tx4 Bias Low Warning	Latched low TX bias warning, channel 4
13	7	L-Tx1 Power High Alarm	Latched high TX Power alarm, channel 1
	6	L-Tx1 Power Low Alarm	Latched low TX Power alarm, channel 1
	5	L-Tx1 Power High Warning	Latched high TX Power warning, channel 1
	4	L-Tx1 Power Low Warning	Latched low TX Power warning, channel 1
	3	L-Tx2Power High Alarm	Latched high TX Power alarm, channel 2
	2	L-Tx2Power Low Alarm	Latched low TX Power alarm, channel 2
	1	L-Tx2Power High Warning	Latched high TX Power warning, channel 2
	0	L-Tx2Power Low Warning	Latched low TX Power warning, channel 2
14	7	L-Tx3Power High Alarm	Latched high TX Power alarm, channel 3
	6	L-Tx3Power Low Alarm	Latched low TX Power alarm, channel 3
	5	L-Tx31 Power High Warning	Latched high TX Power warning, channel 3

	4	L-Tx3Power Low Warning	Latched low TX Power warning, channel 3
	3	L-Tx4Power High Alarm	Latched high TX Power alarm, channel 4
	2	L-Tx4Power Low Alarm	Latched low TX Power alarm, channel 4
	1	L-Tx4Power High Warning	Latched high TX Power warning, channel 4
	0	L-Tx4Power Low Warning	Latched low TX Power warning, channel 4
15-16	All	Reserved	Reserved channel monitor flags, set 4
17-18	All	Reserved	Reserved channel monitor flags, set 5
19-20	All	Reserved	Reserved channel monitor flags, set 6
21	All	Reserved	

Module Monitors

Real time monitoring for the QSFP28 module include transceiver temperature, transceiver supply voltage, and monitoring for each transmit and receive channel. Measured parameters are reported in 16-bit data fields, i.e., two concatenated bytes. These are shown in Table 6.

Table 6 — Module Monitoring Values

Byte	Bit	Name	Description
22	All	Temperature MSB	Internally measured module temperature
23	All	Temperature LSB	
24-25	All	Reserved	
26	All	Supply Voltage MSB	Internally measured module supply voltage
27	All	Supply Voltage LSB	
28-33	All	Reserved	

Channel Monitoring

Real time channel monitoring is for each transmit and receive channel and includes optical input power ，Tx bias current and Tx output Power. Measurements are calibrated over vendor specified operating temperature and voltage and should be interpreted as defined below. Alarm and warning threshold values should be interpreted in the same manner as real time 16-bit data. Table 7 defines the ChannelMonitoring.

Table 7 — Channel Monitoring Values

Byte	Bit	Name	Description
34	All	Rx1 Power MSB	Internally measured RX input power, channel 1
35	All	Rx1 Power LSB	
36	All	Rx2 Power MSB	Internally measured RX input power, channel 2
37	All	Rx2 Power LSB	
38	All	Rx3 Power MSB	Internally measured RX input power, channel 3
39	All	Rx3 Power LSB	
40	All	Rx4 Power MSB	Internally measured RX input power, channel 4
41	All	Rx4 Power LSB	
42	All	Tx1 Bias MSB	Internally measured TX bias, channel 1
43	All	Tx1 Bias LSB	

44	All	Tx2 Bias MSB	Internally measured TX bias, channel 2
45	All	Tx2 Bias LSB	
46	All	Tx3 Bias MSB	Internally measured TX bias, channel 3
47	All	Tx3 Bias LSB	
48	All	Tx4 Bias MSB	Internally measured TX bias, channel 4
49	All	Tx4 Bias LSB	
50	All	Tx1 Power MSB	Internally measured TXoutput power, channel 1
51	All	Tx1 Power LSB	
52	All	Tx2 Power MSB	Internally measured TXoutput power, channel 2
53	All	Tx2 Power LSB	
54	All	Tx3 Power MSB	Internally measured TXoutput power, channel 3
55	All	Tx3 Power LSB	
56	All	Tx4 Power MSB	Internally measured TXoutput power, channel 4
57	All	Tx4 Power LSB	
58-65			Reserved channel monitor set 4
66-73			Reserved channel monitor set 5
74-81			Reserved channel monitor set 6

Control Bytes

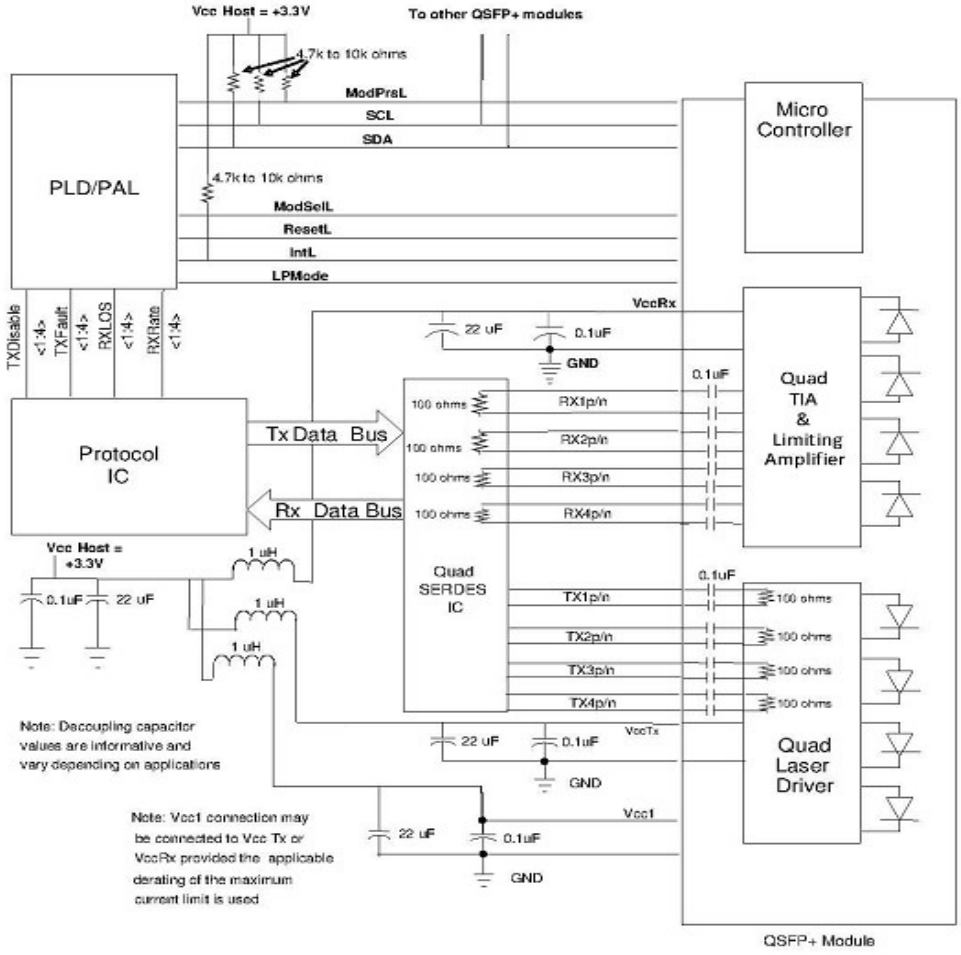
Control Bytes are defined in Table 8

Table 8 — Control Bytes

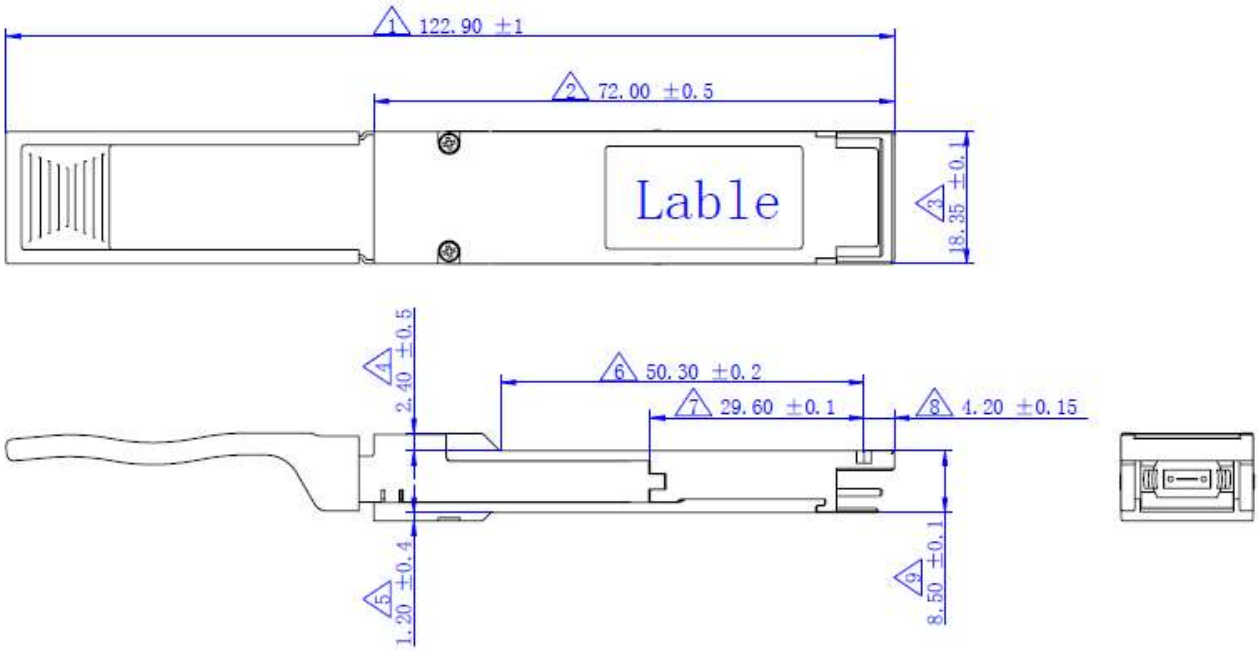
Byte	Bit	Name	Description
86	7-4	Reserved	
	3	Tx4_Disable	Read/write bit that allows software disable of transmitters
	2	Tx3_Disable	Read/write bit that allows software disable of transmitters
	1	Tx2_Disable	Read/write bit that allows software disable of transmitters
	0	Tx1_Disable	Read/write bit that allows software disable of transmitters
87	7	Rx4_Rate_Select	Software Rate Select, Rx channel 4 msb
	6	Rx4_Rate_Select	Software Rate Select, Rx channel 4 lsb
	5	Rx3_Rate_Select	Software Rate Select, Rx channel 3 msb
	4	Rx3_Rate_Select	Software Rate Select, Rx channel 3 lsb
	3	Rx2_Rate_Select	Software Rate Select, Rx channel 2 msb
	2	Rx2_Rate_Select	Software Rate Select, Rx channel 2 lsb
	1	Rx1_Rate_Select	Software Rate Select, Rx channel 1 msb
	0	Rx1_Rate_Select	Software Rate Select, Rx channel 1 lsb
88	7	Tx4_Rate_Select	Software Rate Select, Tx channel 4 msb (Not support)
	6	Tx4_Rate_Select	Software Rate Select, Tx channel 4 lsb (Not support)
	5	Tx3_Rate_Select	Software Rate Select, Tx channel 3 msb (Not support)
	4	Tx3_Rate_Select	Software Rate Select, Tx channel 3 lsb (Not support)
	3	Tx2_Rate_Select	Software Rate Select, Tx channel 2 msb (Not support)
	2	Tx2_Rate_Select	Software Rate Select, Tx channel 2 lsb (Not support)
	1	Tx1_Rate_Select	Software Rate Select, Tx channel 1 msb (Not support)
	0	Tx1_Rate_Select	Software Rate Select, Tx channel 1 lsb (Not support)
89	All	Rx4_Application_Select	Software Application Select per SFF-8079, Rx Channel 4
90	All	Rx3_Application_Select	Software Application Select per SFF-8079, Rx Channel 3
91	All	Rx2_Application_Select	Software Application Select per SFF-8079, Rx Channel 2
92	All	Rx1_Application_Select	Software Application Select per SFF-8079, Rx Channel 1
93	2-7	Reserved	

	1	Power_set	Power set to low power mode. Default 0.
	0	Power_over-ride	Override of LPMode signal setting the power mode with software.
94	All	Tx4_Application_Select	Software Application Select per SFF-8079, Tx Channel 4 (Not support)
95	All	Tx3_Application_Select	Software Application Select per SFF-8079, Tx Channel 3 (Not support)
96	All	Tx2_Application_Select	Software Application Select per SFF-8079, Tx Channel 2 (Not support)
97	All	Tx1_Application_Select	Software Application Select per SFF-8079, Tx Channel 1 (Not support)
98-99	All	Reserved	

Host - Transceiver Interface Block Diagram



Package Outline



Ordering information

Part. No	Specifications								
	Pack	Rate (Gbps)	Tx (nm)	Po (dBm)	RX	Sen (dBm)	Temp (℃)	Reach (m)	DDM
MQBG1D5-DMC-T1	QSFP28	25.78	1310	-9.4~2	PIN	＜-11.5	0~70	500	Y